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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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AMD-MKE C/O FOLEY LARDNER LLP
777 EAST WISCONSIN AVENUE
MILWAUKEE, WI 53202-5306

EXAMINER	
BLUM, DAVID S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/755,746	XIANG, QI	
	Examiner	Art Unit	
	David S. Blum	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *5,13-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-12 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This is in response to the amendment filed 5/27/06.

DETAILED ACTION

Priority

1. This application claims priority as a continuation in part (CIP) to 10/341848, 10/341863, 10/358966, and 10/389456. None of the above priority applications teach or suggest epitaxial growth of a semiconductor or metal directly in contact with the trench sidewalls and in direct contact with the silicon-germanium and strained silicon layers. Thus the document Ohnishi (US007029988B2, US priority date 5/28/03) is applicable.

Double Patenting

2. With the amendment to claims 1, 9, and 17, adding the limitation that a semiconductor or metal directly is epitaxially grown and in contact with the trench sidewalls and in direct contact with the silicon-germanium and strained silicon layers, the double patenting rejection is removed. None of the applications/patents listed in the rejection claim this limitation.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 6, 8-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohnishi (US007029988B2).

Ohnishi teaches all of the positive steps of claims 1-3, 6, and 8-11 as follows.

Regarding claim 1, Ohnishi teaches a method of forming an integrated circuit (column 1 lines 34-35, device is for large scale integration, thus integrated circuits is implied), providing a substrate comprising a silicon-germanium layer (12) and a strained silicon layer (81) above the silicon-germanium layer (see figures 22 and 23), forms a mask layer (83) above the substrate, selectively etches the mask layer to form apertures associated with locations for the trench (22, figure 24), forms trenches (22) having sidewalls (see figure 24 and column 9 line 37), provides a semiconductor or metal layer (261) selectively grown by epitaxy and in direct contact with the trench sidewalls and the silicon-germanium layer and the strained silicon layer (figure 25 and column 9 line 43), and converts the semiconductor or metal layer into oxide liners (column 9 lines 51-52).

Regarding claim 2, an insulative layer (281) is provided to form the trench isolation regions.

The insulative material is removed until the mask layer is reached (figure 28).

Regarding claim 6, the semiconductor or metal layer includes silicon (column 9 lines 42-43).

Regarding claim 8, the formation of the oxide lines is an oxidation process (column 9 lines 49-51).

Regarding claim 9, Ohnishi provides a hard mask layer (83) above a strained semiconductor layer (81), a photoresist layer above the hard mask layer (column 9 lines 25-26, "processed by lithography", thus a photoresist. Column 4 lines 64-67 teaches that Ohnishi includes a photoresist in lithography), selectively removes portions of the photoresist in the photolithographic process (figure 23, part of the hard mask is removed, thus part of the photoresist above was removed), removing the hard mask at locations (figure 23), forming trenches in the strained semiconductor layer (22), providing a conformal semiconductor or metal layer (261) selectively grown by epitaxy and in direct contact with the trench sidewalls and the silicon-germanium layer and the strained silicon layer (figure 25 and column 9 line 43), and oxidizing the semiconductor or metal layer into oxide liners (column 9 lines 51-52).

Regarding claim 10, a pad oxide (82) is provided before providing the hard mask layer.

Regarding claim 11, the pad oxide is removed at the locations before forming the trenches step (figure 23).

Regarding claim 17, Ohnishi forms a liner in a trench by providing a strained layer (81) above a silicon-germanium layer (12), selectively etching (not all material is etched, thus the etch is selective) to form trenches (22), providing a semiconductor (261) in the trench selectively grown by epitaxy and in direct contact with the trench sidewalls and the silicon-germanium layer and the strained silicon layer (figure 25 and column 9 line 43), and converting the semiconductor layer into oxide liners (column 9 lines 51-52). In this embodiment, not all of the semiconductor layer is converted into an oxide. However, in another embodiment where the semiconductor layer is in direct contact with the silicon-germanium and strained silicon layer, Ohnishi teaches the semiconductor layer to be as this as 10 nanometers and up to 10 nanometers is converted to oxide, thus teaching substantially all of the semiconductor layer consumed during the conversion (column 5 lines 10-22).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4 and 7 are is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnishi (US007029988B2) in view of Witek (US 6,146,970).

Ohnishi teaches all of the positive steps of claims 4 and 7 as recited above in regard to claim 1, except for an amorphous capping layer.

Regarding claim 4, Ohnishi teaches a silicon capping layer above the surface as a protection layer. Witek teaches a capping layer of SiN or TEOS (TEOS is amorphous) above the oxide layer to protect the underlying bulk trench fill (column 8 lines 30-50).

Regarding claim 7, Ohnishi teaches a silicon capping layer above the surface (in the fourth embodiment this is above the silicon nitride layer) as a protection layer. Witek teaches a capping layer of SiN or TEOS (TEOS is amorphous) above the oxide layer to protect the underlying bulk trench fill (column 8 lines 30-50).

It would be obvious to one skilled in the requisite art at the time of the invention to modify Ohnishi to have teaches a capping layer of SiN or TEOS (TEOS is amorphous) above the oxide layer as taught by Witek to protect the underlying bulk trench fill (column 8 lines 30-50).

3. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnishi (US007029988B2) in view of Cho (GB 2 254 731 A).

Ohnishi teaches all of the positive steps of claim 12 as recited above in regard to claim 9, except for removing the hard mask in a wet bath.

Regarding claim 12, an insulative material (281) is placed in the trench and the hard mask is removed by wet etching, but does not specifically mention "wet bath". Cho teaches removal of the silicon nitride hard mask by wet etching (a wet bath page 8 lines 15-17). As Cho was published in 1992, it is obvious that wet etching to remove a silicon nitride mask was well known at the time of the invention and one skilled in the requisite art would recognize the two as equivalent arts.

It would be obvious to one skilled in the requisite art at the time of the invention to modify Ohnishi to remove the layer of SiN (hard mask) as taught to be well known by Cho and as such an art recognized equivalent.

4. Claims 18-20 are is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnishi (US007029988B2) Vossen (pages 134, 371, and 336).

Ohnishi teaches all of the positive steps of claims 18-20 as recited above in regard to claim 17, except for epitaxial growth below 600C. and forming the layer by MBE.

Regarding claim 18, Ohnishi teaches forming an epitaxial layer, but does not teach the temperature at which the layer is formed. Vossen teaches epitaxial layers are formed below 800 degrees C. and as low as 550 degrees C. (page 336).

These ranges are considered to involve routine optimization while it has been held to be within the level of ordinary skill in the art. As noted in In re Aller (105 USPQ233), the selection of reaction parameters such as temperature and concentration would have been obvious:

"Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art. Such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."
In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

One skilled in the requisite art at the time of the invention would have used any ranges or exact figures suitable to the method in the process of forming an epitaxial layer regarding temperature using prior knowledge, experimentation, and observation with the apparatus used in order to optimize the process and produce the epitaxial structure desired to the parameters desired.

Regarding claim 19, Ohnishi is silent as to the method used for forming the selective epitaxial layer. Vossen teaches that MBE is a form of selective epitaxial growth (page 371) and teaches MBE has the advantages of low growth temperature that limits diffusion and maintains hyperabrupt interfaces (page 134, 1 of 4 advantages listed).

It would be obvious to one skilled in the requisite art at the time of the invention to modify Ohnishi to use MBE as taught by Vossen to have the advantages of low growth temperature that limits diffusion and maintains hyperabrupt interfaces (page 134, 1 of 4 advantages listed).

Regarding claim 20, Ohnishi teaches the oxide liner to be 1-10 nanometers (column 9 line 20) which is equivalent to 10-100 angstroms (claim limitation is 100-200 angstroms, the ranges over lap).

Response to Arguments

5. Applicant's arguments with respect to claims 1-4, 6-12, and 17-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (571)-272-1687) and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached at (571)-272-1702. Our facsimile number all patent correspondence to be entered into an application is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David S. Blum

August 17, 2006